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Journals

- P. Bhattacharya, R. Bhattacharya, and H. Deka, "MATLAB-Open Source Tool Based Framework for Test Generation for Digital Circuits Using Evolutionary Algorithms". In: Journal of Electronic Testing: Theory and Applications (Springer Nature), vol. 39, no. 5, 2023, DOI: 10.1007/s10836-023-06088-1.
- Rahul Bhattacharya, Subindu Kumar and Santosh Biswas "Fault diagnosis in switched-linear systems by emulation of behavioral models on FPGA: A case study of current-mode buck converter", International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, Wiley. vol. 31, no. 5, pp. 1-27, 2018.
- Rahul Bhattacharya, Subindu Kumar and Santosh Biswas "Resource Optimization for Emulation of Behavioral Models of Mixed Signal Circuits on FPGA: A case study of DC-DC buck converter", International Journal of Circuit Theory and Applications, Wiley, vol. 45, no. 11, pp. 1701-1741, 2017.
- R. Bhattacharya, S. Biswas, S. Mukhopadhyay "FPGA based chip emulation system for test development of analog and mixed signal circuits: A case study of Buck converter", Measurement, Elsevier, vol. 45, issue. 8, pp. 1997-2020, 2012.

Conferences

- Puja Kumari, Rahul Bhattacharya, "MATLAB-Simulink based Framework for Combinational ATPG Applied to Testing of Digital Blocks in Analog and Mixed-Signal Circuits", 28th International Symposium on VLSI Design and Test (VDAT), September 01-03, 2024, Vellore, India. DOI: 10.1109/VDAT63601.2024.10705730
- Abuzar Shakeel, Arpita Dey, Rahul Bhattacharya, Roy Vincent, "Emulation of Nonlinear Dynamics of RF Power Amplifier on FPGA", 9th IEEE International Conference for Convergence in Technology (I2CT), April 05-07, 2024, Page(s): 01-07
- Priyajit Bhattacharya, Abuzar Shakeel, Rahul Bhattacharya, "Fault Emulation in Digital Circuits using FPGA based Software-Hardware Co-Simulation", 11th IEEE International Conference on Signal Processing and Integrated Networks (SPIN), March 21-22, 2024, Page(s): 355-360.
- Rahul Bhattacharya, S.H.M Ragamai, Subindu Kumar, "SFG Based Fault Simulation of Linear Analog Circuits Using Fault Classification and Sensitivity Analysis", 21st International Symposium on VLSI Design and Test (VDAT) 2017, CCIS 711, Springer, pp. 179-190, 2017.
- Anjali Rai, Rahul Bhattacharya, "Parametric Fault Detection for Instrumentation Amplifier Circuit", 2nd IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2016), December 23-25, 2016, Jaipur, India.
- R. Bhattacharya, S. Kumar, "A New Approach for Modeling Parametric Faults in Linear Analog VLSI Circuits", 6th IEEE international conference on Computers and Devices for Communication (CODEC), December 16-18, 2015, DOI: 10.1109/CODEC.2015.7893197
- R. Bhattacharya, S. Biswas, S. Mukhopadhyay "FPGA based Chip Emulation System for Test Development of Analog and Mixed Signal Circuits", 18th annual ACM/SIGDA international symposium on Field programmable gate arrays, 2010, Page: 284.
- M. Rajneesh, R. Bhattacharya, S. Biswas, S. Mukhopadhyay "A NEW APPROACH FOR TESTING OF DIGITAL MODULES IN MIXED SIGNAL VLSI CIRCUITS" IEEE Advanced Computing and Communications, 2007. ADCOM 2007, Page(s): 559-566
- M. Rajneesh, R. Bhattacharya, S. Biswas, S. Mukhopadhyay "A NEW APPROACH FOR TESTING OF DIGITAL MODULES IN MIXED SIGNAL VLSI CIRCUITS", IEEE VLSI Design and Test, 2007, Page(s): 196-204.